3D Integrated LTCC Module using μBGA technology for compact C-band RF Front-End Module

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Abstract: This paper presents a novel 3D integration approach for system-on-package (SOP) based solutions for wireless communication applications. This concept has been applied for the 3D integration of a C band Wireless LAN (WLAN) RF front-end module by means of stacking LTCC substrates using μBGA technology. Characterization and modeling of RF vertical board-to-board transition, using μBGA process are presented for the first time. Specific investigations for 5.8 GHz WLAN applications such as high performance embedded band-pass filter design, and a via-fed stacked cavity-backed patch antenna development are reported. GaAs MESFET-based Rx and Tx chipset is implemented in GaAs MESFET process and combined with the suggested package structure, demonstrate 3D integration concept suitable for C-band wireless communication applications.

I. INTRODUCTION

3D integration approach is a very attractive option to increase density, performance and meet the specifications of the next generation wireless communication systems. Very compact 3D integration technology based on various wafer stacking methods and ultra-thin packaging technology have been successfully proposed for digital applications such as 3D memory and smart cards [1]. However current 3D RF module integration is still based on low density hybrid assembly technologies [2,3]. The development of wireless data communication systems in C-Band leads to very stringent specifications for both IC and packaging performances. For these portable and low-powered applications a high level of integration is also required to reduce essential features as size, weight and interconnection length. Because of the large number of high performance discrete passive components, RF front-end module integration is very challenging. The System-On-Package (SOP) solution (versus the System-On-Chip, SOC), using multi-layer technology has emerged as the most effective approach to achieve simultaneously cost and size reduction, while satisfying the performances and specifications required by these new communication systems. Examples of implementations on both ceramic and organic substrates have been reported [4-5]. Micro ball grid array (μBGA) technology is currently targeted for low cost RF applications and provides great opportunities for 3D integrated RF front-end module [6].

In this paper, we present a very compact 3D-integration concept suitable for C-band RF front-end module by means of LTCC substrate stacking method using μBGA ball process. Characterization of the RF vertical board-to-board transition and an accurate μBGA ball modeling are reported for the first time for RF applications. A high performance second order narrow-band band-pass filter design, with two cascaded coupled line sections, for C-band, and a via-fed stacked cavity-backed patch antenna designed to fully cover the required band (5.725-5.825 GHz), embedded in multiplayer LTCC substrate are presented. GaAs MESFET-based Rx and Tx chipset development is presented, and combined with the suggested package structure.

II. 3D INTEGRATED MODULE CONCEPT.

Figure 1 illustrates the proposed module concept. Two stacked LTCC substrates are used and board-to-board vertical transition is insured by μBGA balls. Standard alignment equipment is used to stack the board and thus provide a compact, high performance and low cost assembly process. Multi-stepped cavities into the LTCC boards provide spacing for embedded RF active devices and thus lead to significant volume reduction by minimizing the gap between the boards. Active devices can be flip-chiped as well as wire-bonded. Cavities provides also integration opportunity for MEMSs devices such as MEMS Switch. Passive components, off-chip matching networks, embedded filter and antenna are implemented directly into the LTCC boards by using multi-layer technology [4]. Standard BGA balls insure interconnection of this high density module with a mother board such as FR4 board. The top and the bottom substrates are dedicated respectively to the receiver and transmitter building blocks of the RF front-end module. Figure 2 shows the block diagram of each board. The receiver board includes antenna, band-pass filter, active Switch, LNA, VCO and Down-conversion Mixer. The Transmitter board includes Up-conversion Mixer, PA and

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off-chip matching networks. Ground planes and vertical via walls [7] are used to address isolation issues between the transmitter and the receiver functional blocks. Arrays of vertical via are added into the transmitter board to achieve better thermal management.

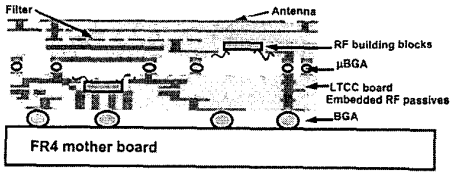


Fig. 1. 3D integrated module concept view.

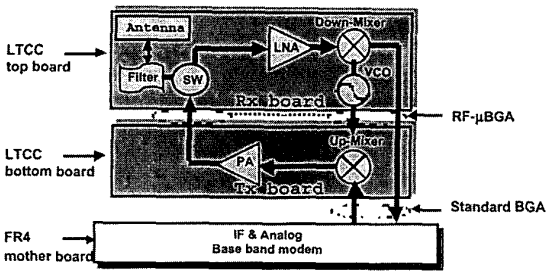


Fig. 2. Rx and Tx board block diagram.

III. CHARACTERIZATION AND MODELLING OF THE BOARD TO BOARD TRANSITION.

Special care is required in the board-to-board transition to maintain ground, 50-Ohms matching continuity and address coupling and resonance issues. It has been shown that CPW line is the best configuration to avoid vertical coupling between the board and the IC in BGA and flip-chip technology [8]. However the significant reduction of the gap between the two stacked boards, caused by using µBGA ball process, arouses the need of modified CPW design. An accurate model for the µBGA balls is also required to optimize the RF vertical transition design. Figure 3 describes the three structures witch have been designed for the characterization of µBGA balls. Thin film metal (Au) is deposited on the top and bottom LTCC boards and then photo-patterned and etched to form the circuitry. 4 mils diameter µBGA solder balls (Sn63Pb37-183°C), standard alignment equipment and conventional reflow process (maximum temperature: 230 °C) have been used to stack the board. Both TRL calibration and TLL de-embedding techniques proposed in [8] have been used to extract S-parameters of the CPW line. Afterwards, these parameters and the overall measurement data have been inserted into a circuit schematic in HP-ADS. Using a fitting-to-measurement method, we have set up a modified model for the CPW and developed a hybrid equivalent circuit model for the µBGA RF transition.

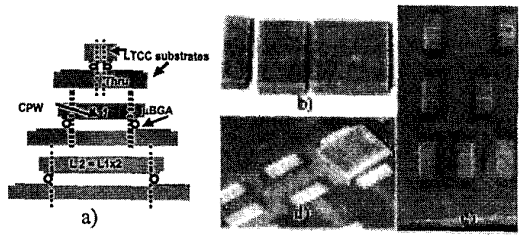


Fig. 3. Board-to-board transition test structures schematic (a) photos of the top (b), bottom (c) and stacked (d) substrates.

Figure 4 demonstrates the effects of the modification into the model to obtain the accurate CPW behavior. A combination of RLC ∏-network and transmission line model is applied to model the µBGA ball. In figure 5a, C represents the effect from the metalization overlap area, R accounts for the parasitic resistance and L the inductance for the self inductance of the balls. The two transmission line sections are added to model accurately the phase responses of S11 and S21. This model predicts insertion loss less than 0.1 dB and return loss about - 17dB up to 10 GHz. Figure 5b shows the extracted performances of a single ball transition. Post full wave simulations have also been performed to validate the developed models.

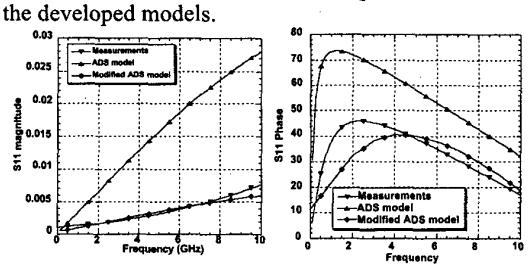


Fig. 4. Modified CPW model.

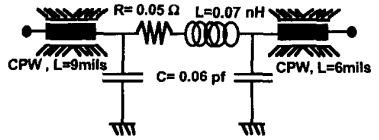


Fig. 5a. Extracted µBGA hybrid model

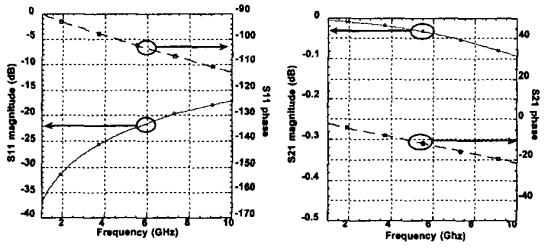


Fig. 5b. Extracted µBGA S-parameters.

IV. LTCC BOARD DEVELOPMENT

We have first focused our studies on the receiver board. In order to predict the module performances, an accurate modeling and optimization of the whole package is required. All the packaging elements along the RF path have to be considered, namely the RF input and output pads, embedded filter, multiple stacked vertical via, transition between different types of transmission lines, material discontinuity, wire-bonding. The module design is based on a 10 layers LTCC process whose the main features are described in Table 1. Copper metalization and filled vertical via technologies are used to improve electrical performances.

TABLE 1: LTCC process features.

ε_r	Tan δ	Dielectric Thickness	Line width And spacing	Via diameter
5.8	1.2e-3	4 mils	4mils	4 mils

We've assigned each layer as following: layer 1 to 5 are dedicated for the embedded filter and layer 6 to 10 are dedicated for vertical interconnections and multi-stepped cavities design. Total size of the receiver board, including the RF chipset, is 7.8 x 6 x 0.9mm^3.

A. Embedded Band-pass filter

We have developed a high performance second order narrow-band band-pass filter with two cascaded coupled line sections embedded in strip-line configuration to improve insertion loss. A schematic view is presented in figure 6. Coupled lines have been bent to fit into the module shape and via walls are used to connect ground planes and reduce parallel plate modes. Filter performances has been measured separately and exhibit a –2.9dB insertion loss, – 20.8dB return loss, about 200 MHz bandwidth and image rejection greater than –20 dB as shown in figure 7.

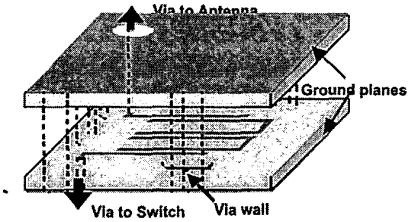


Fig. 6. Band-pass filter design schematic view.

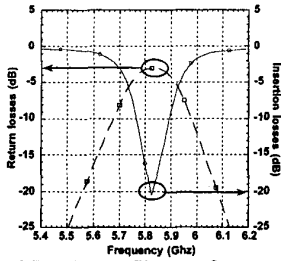


Fig. 7.: Measured Band-pass filter performances.

B. Embedded Antenna

A via-fed stacked cavity-backed patch antenna has been designed for IEEE 802.11a 5.8 GHz band as shown in Fig. 8. The heights of the lower and upper patches (400 mils × 400 mils) are respectively 8 mils (2 LTCC GL550 layers) and 32 mils.

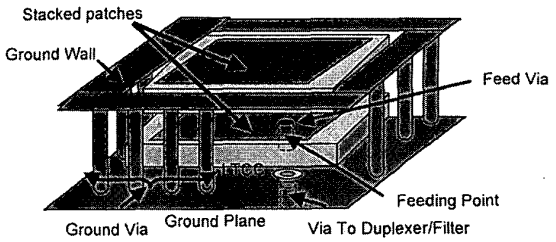


Fig. 8. Stacked patch antenna for IEEE 802.11a 5.8 GHz band.

The input impedance characteristic of the stacked-patch antenna is shown in Fig. 9. The 10-dB return-loss bandwidth of the antenna is about 4%, fully covering the required band (5.725-5.825 GHz). Also this antenna has a desirable gain (near 6 dBi) and very low cross-polarization (less than –35 dBi).

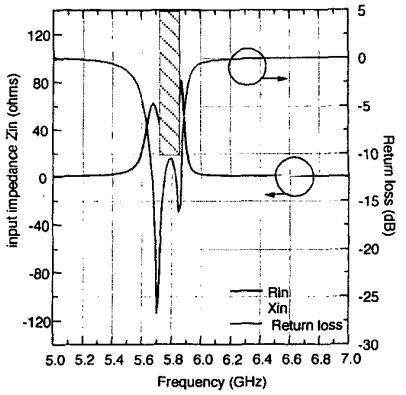
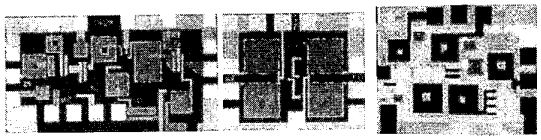


Fig. 9. Input impedance characteristic of the stacked patch antenna for IEEE 802.11a 5.8 GHz band.

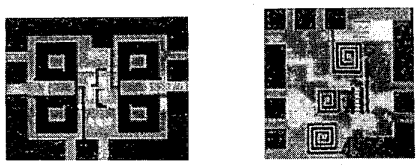
V. RX & TX CHIPSET DEVELOPMENT.

We used commercial 0.6um GaAs MESFET process to implement Rx and Tx chipset. Rx chipset consists in LNA, down converter mixer, and VCO as shown in Figure 10. Tx chipset includes double balanced diode ring mixer and RF amplifier as shown in Figure 11.



(a) (b) (c)

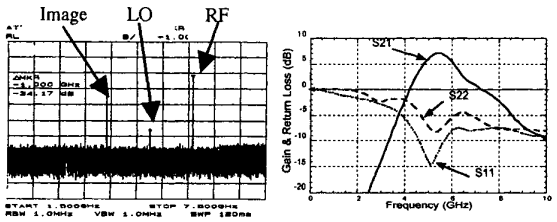
Fig. 10. Photo of the Rx chipset used in the module (a) LNA (b) Mixer (c) VCO



(a) (b)

Fig. 11. Photo of the Tx chipset used in the module (a) Mixer (b) RF amplifier

The LNA gain is about 13, the LNA noise is about 2.2 dB. Figure 13 (a) shows the output spectrum of the transmitter mixer demonstrating image signal rejection of 11 dBc, and LO-to-RF rejection of 40 dB, across the VCO tuning range between 4.5 GHz to 5.5 GHz. It also shows less than 11 dB conversion loss between IF frequency from DC to 1 GHz. The RF amplifier demonstrates a measured gain of 7 dB and 1-dB compression point of 17 dBm as shown in Figure 13 (b).



(a) (b)

Fig. 13. Tx module performances (a) Mixer output spectrum (b) RF amplifier gain

VI. CONCLUSION

We have presented a very compact 3D-integration concept, based on two stacked LTCC substrates connected by means of μBGA balls. Characterization of the board-to-board transition and an accurate μBGA ball modeling are reported for the first time in RF applications. A high performances second order narrow-band band-pass filter with two cascaded coupled line sections has been presented. A via-fed stacked cavity-backed patch antenna has been designed to fully cover the required band (5.725-5.825 GHz) and implemented in multiplayer LTCC substrate. A GaAs MESFET-based (0.6um process) Rx and Tx chipset was implemented, combined with the suggested package structure, demonstrate 3D integration concept suitable for C-band wireless communication applications. The proposed concept is also applicable to others telecommunications systems towards more miniaturization.

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